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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GARCIA OTERO, EDUARDO	

ART UNIT	PAPER NUMBER
2123	17

DATE MAILED: 01/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/649,437	REYNOLDS ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION: Non-Final

Introduction

1. Title is: METHOD AND APPARATUS FOR SPECIFYING ADDRESSABILITY AND BUS CONNECTIONS IN A LOGIC DESIGN
2. First named inventor is: REYNOLDS
3. Applicant has submitted an Information Disclosure Statement, and Request for Continued Examination, and Amendment B received 8/25/03 (amending claims 1, 2, 10, 11). Applicant also requested a one month suspension. The period for suspension has expired.
4. Claims 1-29 have been submitted, examined, and rejected.
5. This is the first action on the merits after Request for Continued Examination, and is non-final.

Index

6. **Tabak** refers to Advanced Microprocessors, by Daniel Tabak, McGraw-Hill, Inc., ISBN: 0-07-062843-2, 1995.
7. **Microsoft Computer Dictionary** refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.
8. **McGraw-Hill Dictionary** refers to The McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, by McGraw-Hill Companies, Inc., ISBN 0-07-042313-X, 2003.
9. **Dangelo'678** refers to US Patent 6,324,678.

Filing date-priority

10. The Examiner notes that the petition to correct filing date was granted, and that the correct filing date is 8/23/00. No earlier priority is claimed.

Specification-objections-WITHDRAWN

11. The Applicant has amended the specification to describe the lines/inputs in FIGS 2-4. The prior objection is withdrawn.

Remarks (definitions)

12. DATA ACCESS PRIMITIVES. There are at least 4 possible definitions for this term.

13. First definition, Specification page 7 line 4 states "The logic designer uses a set of logic design components, referred to herein as "data access primitives", to specify an assembly of address and lane-matching logic and associated data bus connections. The data access primitive hides the details of interconnection to the bus, and abstracts away the interdependency of address-matching functions, lane-matching functions, and data bus connections."
14. Note that "hides the details" appears to imply that the details exist, but are simply not being shown. Similarly, "abstracts away the interdependency" appears to imply that the interdependency exists, or existed, and that the "data access primitive" goes from a low level of abstraction which contains the interdependency, to a high level of abstraction which removes ("abstracts away") the interdependency. However, in the context of the whole specification, it appears that the "data access primitives" are used before the details of interconnection and interdependencies are defined. Thus, the Specification page 7 line 4 definition appears inconsistent with the remainder of the specification.
15. Second definition, Applicant Remarks page 11 states "data access primitives are logic design components that may be used by a designer to specify an assembly of address and lane matching logic". This statement does not clarify the definition in the specification, but merely repeats a portion of the definition in the specification. Remarks page 12 states "Further, each data access primitive implies address-matching functions, lane-matching functions, data bus connections...". It is not clear what the Applicant intends by the Remarks page 12 term **"implies** address-matching functions". Specifically, it is not clear how a "logic design component" can "imply" an address-matching function. Thus, the Remarks page 12 discussion is not clear.
16. Third definition, the McGraw-Hill Dictionary defines "primitive" as "[COMPUT SCI] A sketchy specification, omitting details, of some action in a computer program". This definition appears to be reasonably close to the way "data access primitive" is used in the specification. In particular, "omitting details" appears more accurate than the specification page 7 term "hiding details".
17. Fourth definition, Microsoft Computer Dictionary Fourth Edition defines "primitive" as "1. In computer graphics, a shape, such as a line, circle, curve, or polygon, that can be

drawn, stored, manipulated as a discrete entity by a graphics program. A primitive is one of the elements from which a large graphic design is created. 2. In programming, a fundamental element in a language that can be used to create larger procedures that do the work a programmer wants to do". This Microsoft definition does not appear as relevant as the McGraw-Hill definition above.

18. In view of the specification as a whole including the above 4 definitions, **the examiner interprets "data access primitive" as "logic design components that omit details of interconnection to bus, and omit interdependencies of address matching functions, lane-matching functions, and data bus connections".** By "omit", the Examiner means "does not contain".
19. The 35 USC 103 rejections have been amended to include Dangelo'678 as prior art, see below.

35 USC § 112-Second Paragraph-indefinite claims

20. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
21. **Claims 1-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
22. In claim 1, the term **"data access primitive"** is indefinite. Applicant variously describes said term as: "hides the details... abstracts away the interdependencies" at Specification page 7 line 4, and "implies address-matching functions..." at Remarks page 12. It is not clear how said "data access primitive" hides or abstracts or implies said details and interdependencies and functions.
23. Also in claim 1, the first limitation states "using a data primitive to model addressability for a memory-mapped device, addressability comprising an address matching function, a lane matching function and one or more bus connections". It is not clear how said "data access primitive" can "model" said "address matching function..." while hiding or abstracting the details and interdependencies. Claims 2-29 are indefinite for the same reasons.

Claim Interpretation

24. The claim language is interpreted in light of the specification. Limitations from the specification must not be imported into the claims, but definitions from the specification must be imported into the claims.

25. The Examiner hereby interprets **"data access primitive" as "logic design components that omit details of interconnection to bus, and omit interdependencies of address matching functions, lane-matching functions, and data bus connections".** By "omit", the Examiner means "does not contain". See above detailed discussion in Remarks section.

35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

> Determining the scope and contents of the prior art.
> Ascertaining the differences between the prior art and the claims at issue.
> Resolving the level of ordinary skill in the pertinent art.
> Considering objective evidence present in the application indicating obviousness or nonobviousness.

28. Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable.

29. Claim 1 (presently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Tabak.

30. Claim 1 (presently amended) is an independent method claim with 6 limitations, labeled by the Examiner for clarity.

31. Applicant has amended "converting the data access primitive to logic components that implement a first set of addressing matching function..." to read "replacing the data access primitive with logic components that implement..."

32. [1] **"using a data access primitive"** is disclosed by Dangelo'678 Abstract "A methodology for generating structural descriptions of complex digital devices from **high-level descriptions and specifications** is disclosed. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level descriptions. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals" (emphasis added), and FIG 16a "HIGHEST LEVEL" and "MEDIUM-HIGH" levels of abstraction, and column 22 line 13 "Top-Down Design Methodology".
33. The remaining additional limitations are not expressly disclosed by Dangelo'678.
34. [2] **"an address matching function"** is disclosed by Tabak at page 48 "Address mapping".
35. [3] **"a lane matching function"** is disclosed by Tabak at page 4 Table 1.1. Note that the following Intel microprocessors have a small external databus and a large internal databus: 8088, 80188, 80376. The Examiner has taken the liberty of expanding Table 1.1 with the information from page 5 in order to make this point clear. The small external databus (half the size of the internal databus) is used to reduce costs associated with external processes, see Tabak page 5.
36. These microprocessors inherently lane match, because input data from the small external databus must be matched to the proper lane of the large internal databus. For example, in the 8088, during one clock cycle, 8 bits from the small external databus are placed in the first lane of the 16 bit large internal databus, and during the next clock cycle another 8 bits from the small external databus are placed in the second lane of the 16 bit large internal databus.
37. [4] **"one or more bus connections"** is disclosed by Tabak at page 5 "internal databus" and "external databus".
38. [5] **"specifying a first starting address for the memory-mapped device"** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping".

39. [6] "**generating a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device using the data access primitive and the first starting address**" is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.
40. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tabak to modify Dangelo'678. One of ordinary skill in the art, starting with Dangelo's high level abstraction description, would have been motivated use Tabak's modern address matching and lane matching functions in order to connect buses of different sizes, and/or components of different sizes.
41. Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Tabak and Applicant's Admission and MPEP 2144.04 (Routine Expedient of making automatic).
42. Claims 2-9 depend from claim 1, with the following additional limitations.
43. In claim 2, "**replacing the data access primitive with logic components that implement a second set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device using the data access primitive and a second starting address**" is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line k through Line 2k of the Main Memory.
44. In claim 3, "**coupling the data access primitive to the memory-mapped device**" is disclosed by Tabak at Figure 4.4 "Cache-memory mapping".
45. Also in claim 3, "**coupling an address bus to the data access primitive**" is disclosed by Tabak at Figure 4.4 "Cache-memory mapping".
46. In claim 4, "**the addressing matching function compares an address from the address bus with the first starting address for the memory-mapped device**" is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.
47. In claim 5, "**the first starting address is specified by a user**" is disclosed by Applicant's Admission at specification background page 1 line 23 "specifying the addressability and bus connections may be tedious", and page 2 lines 3-5

"interdependencies... make it much more likely that the logic designer will accidentally specify inconsistent addressability and bus connection information".

48. Regarding admissions, MPEP § 2129 states "When applicant states that something is prior art, it is taken as being available as prior art against the claims". *In re Nomiya*, 509 F.2d 566, 184 USPQ 607, 611 (CCPA 1975) states "admissions...may be considered "prior art" for any purpose, including use as evidence of obviousness under § 103". *Constant v. Advanced Micro-Devices,* 848 F2d 1560, 1570, 7 USPQ2d 1057, 1063 (Fed. Cir. 1988), "[Applicant's] own admission during prosecution...is binding upon him". Additionally, U.S. Patent and Trademark Office (USPTO), Formulating and Communicating Rejections Under 35 U.S.C. 1037 (Feb. 13, 1991) states when relying on an admission as evidence of obviousness, moreover, it is unnecessary to cite a corroborating reference to support the admission. Also see 37 C.F.R. § 1.104(c)(3).
49. In claim 6, **"the first starting address is generated automatically"** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11. Also, *In re Venner*, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Additionally, MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art."
50. In claim 7, **"the first starting address is generated automatically using a set of address constraints"** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.
51. In claim 8, **"addressability for a minimum size transaction supported by the memory-mapped device"** is disclosed by Tabak at page 4 Table 1.1. Note that the following Intel microprocessors have a small external databus and a large internal databus: 8088, 80188, 80376. The Examiner has taken the liberty of expanding Table 1.1 with the information from page 5 in order to make this point clear. The small

external databus (half the size of the internal databus) is used to reduce costs associated with external processes, see Tabak page 5.

52. In claim 9, **"the memory-mapped device is a register"** is disclosed by Tabak at page 9 Figure 2.1 "Floating Point Register File (FRF)".
53. MOTIVATION FOR DEPENDENT CLAIMS 2-9. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tabak and Applicant's Admission and *In re Venner* to modify Dangelo'678. One of ordinary skill in the art, starting with Dangelo's high level abstraction description, would have been motivated use Tabak's modern address matching and lane matching functions in order to connect buses of different sizes, and/or components of different sizes to "fully specify the addressability and bus connections of the memory-mapped devices" according to specification background page 1 line 11. Additionally, one of ordinary skill in the art would be motivated and to save time and money and reduce errors by automating (per *In re Venner*) the addressability according to specification background page 1 line 23 "tedious" and specification page 2 line 5 "accidentally specify inconsistent addressability".
54. Claim 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Tabak and Applicant's Admission and MPEP 2144.04 (Routine Expedient of making automatic).
55. Claims 10-17 are computer readable medium claims with the same limitations as method claims 1-8 respectively, and thus are rejected for the same reasons.
56. Claim 18 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Tabak.
57. Claim 18 (amended) is an independent method claim, with 9 limitations.
58. [1] **"selecting a data access primitive"** is disclosed by Dangelo'678 Abstract "A methodology for generating structural descriptions of complex digital devices from **high-level descriptions and specifications** is disclosed. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level descriptions. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level,

the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals" (emphasis added), and FIG 16a "HIGHEST LEVEL" and "MEDIUM-HIGH" levels of abstraction, and column 22 line 13 "Top-Down Design Methodology".

59. The remaining additional limitations are not expressly disclosed by Dangelo'678.
60. [2] **"an addressing matching function"** is disclosed by Tabak at page 48 "Address mapping".
61. [3] **"lane matching function"** is disclosed by Tabak at page 4 Table 1.1. Note that the following Intel microprocessors have a small external databus and a large internal databus: 8088, 80188, 80376. The Examiner has taken the liberty of expanding Table 1.1 with the information from page 5 in order to make this point clear. The small external databus (half the size of the internal databus) is used to reduce costs associated with external processes, see Tabak page 5.
62. These microprocessors inherently lane match, because input data from the small external databus must be matched to the proper lane of the large internal databus. For example, in the 8088, during one clock cycle, 8 bits from the small external databus are placed in the first lane of the 16 bit large internal databus, and during the next clock cycle another 8 bits from the small external databus are placed in the second lane of the 16 bit large internal databus.
63. [4] **"one or more bus connections for a memory-mapped device"** is disclosed by Tabak at page 5 "internal databus" and "external databus".
64. [5] **"specifying an address constraint for the memory-mapped device"** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.
65. [6] **"generating a starting address for the memory mapped device using the address constraint"** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.
66. [7] **"generating the address matching function"** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see

"memory management unit (MMU)" at page 11.

67. [8] **"generating the lane matching function"** is disclosed by Tabak at page 4 Table 1.1. Note that the following Intel microprocessors have a small external databus and a large internal databus: 8088, 80188, 80376. The Examiner has taken the liberty of expanding Table 1.1 with the information from page 5 in order to make this point clear. The small external databus (half the size of the internal databus) is used to reduce costs associated with external processes, see Tabak page 5.
68. [9] **"the one or more bus connections"** is disclosed by Tabak at page 5 "internal databus" and "external databus".
69. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tabak to modify Dangelo'678. One of ordinary skill in the art, starting with Dangelo's high level abstraction description, would have been motivated to use Tabak's modern address matching and lane matching functions in order to connect buses of different sizes, and/or components of different sizes.
70. Claims 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Tabak and Applicant's Admission and MPEP 2144.04 (Routine Expedient of making automatic).
71. Dependent claims 19-23 depend from claim 18.
72. In claim 19, **"the address constraint is specified by a user"** is disclosed by Applicant's Admission at specification background page 1 line 23 "specifying the addressability and bus connections may be tedious", and page 2 lines 3-5 "interdependencies... make it much more likely that the logic designer will accidentally specify inconsistent addressability and bus connection information".
73. Also in claim 19, **"the starting address for the memory mapped device"** is disclosed by Applicant's Admission at specification background page 1 line 23 "specifying the addressability and bus connections may be tedious", and page 2 lines 3-5 "interdependencies... make it much more likely that the logic designer will accidentally specify inconsistent addressability and bus connection information".
74. Additionally in claim 19, **"[the starting address for the memory mapped device] is generated automatically"** is disclosed by *In re Venner* (legal precedent for making

automatic). *In re Venner,* 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Additionally, MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art." Here, by Applicant's admission, at specification background page 1 line 15-18 "Traditional electronic design automation tool flows require the addressability and data connections of a device to a system bus to be explicitly specified [by the designer]. This includes address matching, lane matching, connection to system bus data bits and any other auxiliary logic." Thus, generating the starting address automatically merely replaces "manual activity [by the designer] which has accomplished the same result".

75. In claim 20, **"the transaction size is one in a group comprising a byte, a halfword and a word"** is disclosed by Tabak at page 21 "byte", "halfword", and "word".
76. In claim 21, **"using a new starting address for the memory-mapped device without having to specify changes to the addressing function, the lane matching function and the one or more bus connections"** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line k through Line 2k of the Main Memory.
77. In claim 22, **"a different logic for the memory mapped device is instantiated automatically using the same data access primitive and the new starting address"** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line k through Line 2k of the Main Memory.
78. In claim 23, **"the addressing matching function compares an address from an address bus coupled with the data access primitive with the starting address, and wherein when there is match, the lane matching function matching the transaction size of a transaction to a respective section of the memory-mapped device"** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line k through Line 2k of the Main Memory.
79. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Tabak and Applicant's Admission and MPEP 2144.04 (Routine Expedient of making automatic) to modify Dangelo'678. One of ordinary skill in the art

would have been motivated to do this because it is required to "fully specify the addressability and bus connections of the memory-mapped devices" according to specification background page 1 line 11, and to save time and money and reduce errors by automating the addressability according to specification background page 1 line 23 "tedious" and page 2 line 5 "accidentally specify inconsistent addressability".

80. Claim 24 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Tabak.
81. Claim 24 is computer readable medium claim with the same limitations as method claims 18, and thus is rejected for the same reasons.
82. Claims 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Tabak and Applicant's Admission and MPEP 2144.04 (Routine Expedient of making automatic).
83. Claims 25-29 are computer readable medium claims with the same limitations as method claims 19-23 respectively, and thus are rejected for the same reasons.

Conclusion

84. All pending claims 1-29 stand rejected.

Communication

85. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER